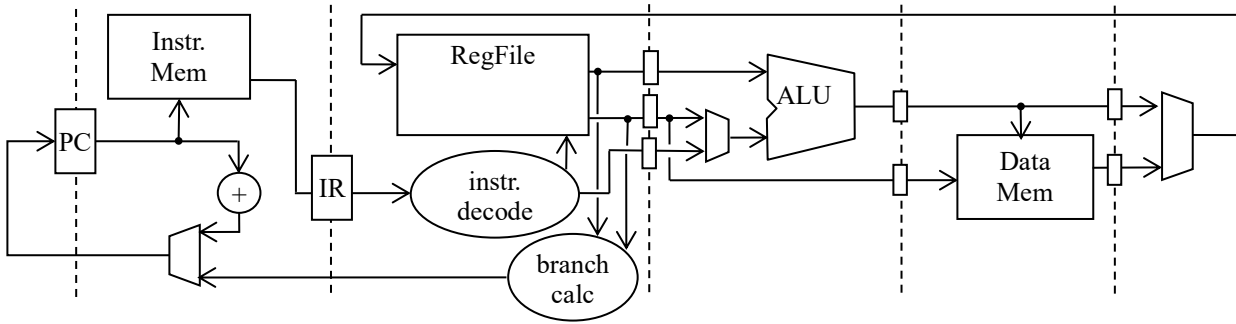


Simplified 5-stage pipelined MIPS datapath. Dashed lines indicate boundaries between pipeline stages.
Note: In this version, PC calculations for jumps and branches are performed during the second stage.



Units and conversions

- 1 KB = 1024 bytes = 2^{10} bytes \approx one thousand bytes
- 1 MB = 1024 KB = 1024×1024 bytes = 2^{20} bytes \approx one million bytes
- 1 GB = 1024 MB = $1024 \times 1024 \times 1024$ bytes = 2^{30} bytes \approx one billion bytes
- 1 GHz = 1,000,000,000 cycles/second = 1 billion cycles / second = 1 cycle / ns
- 1 MHz = 1,000,000 cycles/second = 1 million cycles / second = 1 cycle / μ s
- 1 KHz = 1,000 cycles/second = 1 thousand cycles / second = 1 cycle / ms
- 1 ps = 1 picosecond = one trillionth of a second
- 1 ns = 1 nanosecond = one billionth of a second = 1000 ps
- 1 μ s = 1 microsecond = one millionth of a second = 1000 ns
- 1 ms = 1 millisecond = one thousandth of a second = 1000 μ s

ASCII Table

Dec	Hex	Ascii	Dec	Hex	Ascii	Dec	Hex	Ascii	Dec	Hex	Ascii
0	00	'\0'	32	20	' ' (space)	64	40	@	96	60	`
1	01	SOH	33	21	!	65	41	A	97	61	a
2	02	STX	34	22	"	66	42	B	98	62	b
3	03	ETX	35	23	#	67	43	C	99	63	c
4	04	EOT	36	24	\$	68	44	D	100	64	d
5	05	ENQ	37	25	%	69	45	E	101	65	e
6	06	ACK	38	26	&	70	46	F	102	66	f
7	07	'\a' (bell)	39	27	'	71	47	G	103	67	g
8	08	'\b' (backspace)	40	28	(72	48	H	104	68	h
9	09	'\t' (tab)	41	29)	73	49	I	105	69	i
10	0A	'\n' (newline)	42	2A	*	74	4A	J	106	6A	j
11	0B	'\v' (vtab)	43	2B	+	75	4B	K	107	6B	k
12	0C	'\f' (formfeed)	44	2C	,	76	4C	L	108	6C	l
13	0D	'\r'	45	2D	-	77	4D	M	109	6D	m
14	0E	SO	46	2E	.	78	4E	N	110	6E	n
15	0F	SI	47	2F	/	79	4F	O	111	6F	o
16	10	DLE	48	30	0	80	50	P	112	70	p
17	11	DC1	49	31	1	81	51	Q	113	71	q
18	12	DC2	50	32	2	82	52	R	114	72	r
19	13	DC3	51	33	3	83	53	S	115	73	s
20	14	DC4	52	34	4	84	54	T	116	74	t
21	15	NAK	53	35	5	85	55	U	117	75	u
22	16	SYN	54	36	6	86	56	V	118	76	v
23	17	ETB	55	37	7	87	57	W	119	77	w
24	18	CAN	56	38	8	88	58	X	120	78	x
25	19	EM	57	39	9	89	59	Y	121	79	y
26	1A	SUB	58	3A	:	90	5A	Z	122	7A	z
27	1B	ESC	59	3B	;	91	5B	[123	7B	{
28	1C	FS	60	3C	<	92	5C	\	124	7C	
29	1D	GS	61	3D	=	93	5D]	125	7D	}
30	1E	RS	62	3E	>	94	5E	^	126	7E	~
31	1F	US	63	3F	?	95	5F	_	127	7F	DEL

Num	Name	Description
r0	\$zero	zero
r1	\$at	assembler temp
r2	\$v0	function
r3	\$v1	return values
r4	\$a0	function
r5	\$a1	arguments
r6	\$a2	(first 4, also
r7	\$a3	space on stack)
r8	\$t0	temps (caller save)
r9	\$t1	
r10	\$t2	
r11	\$t3	
r12	\$t4	
r13	\$t5	
r14	\$t6	
r15	\$t7	

Num	Name	Description	
r16	\$s0	saved (callee save)	
r17	\$s1		
r18	\$s2		
r19	\$s3		
r20	\$s4		
r21	\$s5		
r22	\$s6		
r23	\$s7		
r24	\$t8		more temps (caller save)
r25	\$t9		
r26	\$k0	reserved for OS kernel	
r27	\$k1		
r28	\$gp	global pointer	
r29	\$sp	stack pointer	
r30	\$fp/s8	frame pointer	
r31	\$ra	return address	

Num	Name	Description
hi		products & quotients
lo		
pc		program counter
ir		instruction register

Notation	Description
SE(x)	x, sign-extended
ZE(x)	x, zero-extended
LB(x)	low byte of x
LH(x)	low half of x
MEM[x]:n	n bytes at address x
hi:lo	hi and lo, joined
<<	left shift
>>	right shift, arithmetic
>>>	right shift, zero extend

Arithmetic Instructions

Instruction	Operation
addu \$d, \$s, \$t	\$d = \$s + \$t
addiu \$t, \$s, imm	\$t = \$s + SE(imm)
subu \$d, \$s, \$t	\$d = \$s - \$t
xor \$d, \$s, \$t	\$d = \$s ^ \$t
and \$d, \$s, \$t	\$d = \$s & \$t
andi \$t, \$s, imm	\$t = \$s & ZE(imm)
div \$s, \$t	lo = \$s / \$t; hi = \$s % \$t
divu \$s, \$t	lo = \$s / \$t; hi = \$s % \$t
mult \$s, \$t	hi:lo = \$s * \$t
multu \$s, \$t	hi:lo = \$s * \$t
nor \$d, \$s, \$t	\$d = ~(\$s \$t)
or \$d, \$s, \$t	\$d = \$s \$t
ori \$t, \$s, imm	\$t = \$s ZE(imm)
sll \$d, \$t, amt	\$d = \$t << amt
sllv \$d, \$t, \$s	\$d = \$t << \$s
sra \$d, \$t, amt	\$d = \$t >> amt
srav \$d, \$t, \$s	\$d = \$t >> \$s
srl \$d, \$t, amt	\$d = \$t >>> amt
srlv \$d, \$t, \$s	\$d = \$t >>> \$s
lui \$d, imm	\$d = imm << 16

Special Register Instructions

mfhi \$d	\$d = hi
mflo \$d	\$d = lo

Pseudo-Instructions

li \$d, imm	\$d = imm
la \$d, label	\$d = addr of label
move \$d, \$t	\$d = \$t
div \$d, \$s, \$t	\$d = \$s / \$t
mul \$d, \$s, \$t	\$d = \$s * \$t
mod \$d, \$s, \$t	\$d = \$s % \$t
nop	no operation

Comparison Instructions

Instruction	Operation
slt \$d, \$s, \$t	\$d = (\$s < \$t)
sltu \$d, \$s, \$t	\$d = (\$s < \$t)
slti \$t, \$s, imm	\$t = (\$s < SE(imm))
sltiu \$t, \$s, imm	\$t = (\$s < ZE(imm))

Note: Comparisons set destination register to 1 (true) or 0 (false).

Branch Instructions & Pseudo-Instructions

beq \$s, \$t, label	if (\$s==\$t) pc+=4+SE(imm)<<2
bne \$s, \$t, label	if (\$s!=\$t) pc+=4+SE(imm)<<2
bgt \$s, \$t, label	if (\$s>\$t) pc+=4+SE(imm)<<2
blt \$s, \$t, label	if (\$s<\$t) pc+=4+SE(imm)<<2
bge \$s, \$t, label	if (\$s>=\$t) pc+=4+SE(imm)<<2
ble \$s, \$t, label	if (\$s<=\$t) pc+=4+SE(imm)<<2
bgtz \$s, label	if (\$s>0) pc+=4+SE(imm)<<2
bltz \$s, label	if (\$s<0) pc+=4+SE(imm)<<2
bgez \$s, label	if (\$s>=0) pc+=4+SE(imm)<<2
blez \$s, label	if (\$s<=0) pc+=4+SE(imm)<<2

Jump Instructions

j label	pc = SE(imm) << 2
jal label	\$31 = pc; pc = SE(imm)<<2
jalr \$s	\$31 = pc; pc = \$s
jr \$s	pc = \$s

Note: Jumps with an immediate retain the top 4 bits of pc+4.

Load/Store Instructions

lb \$t, imm(\$s)	\$t = SE(MEM[\$s + SE(imm)]:1)
lbu \$t, imm(\$s)	\$t = ZE(MEM[\$s + SE(imm)]:1)
lh \$t, imm(\$s)	\$t = SE(MEM[\$s + SE(imm)]:2)
lhu \$t, imm(\$s)	\$t = ZE(MEM[\$s + SE(imm)]:2)
lw \$t, imm(\$s)	\$t = MEM[\$s + SE(imm)]:4
sb \$t, imm(\$s)	MEM[\$s + SE(imm)]:1 = LB(\$t)
sh \$t, imm(\$s)	MEM[\$s + SE(imm)]:2 = LH(\$t)
sw \$t, imm(\$s)	MEM[\$s + SE(imm)]:4 = \$t